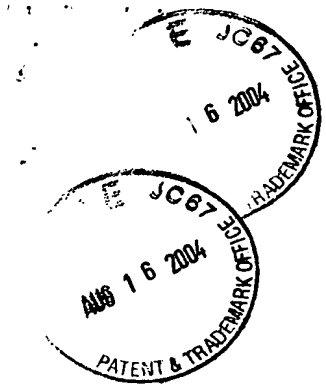

UNITED STATES PATENT AND TRADEMARK OFFICE

I, Susan ANTHONY BA, ACIS,

Director of RWS Group plc, of Europa House, Marsham Way, Gerrards Cross, Buckinghamshire, England declare;

1. That I am a citizen of the United Kingdom of Great Britain and Northern Ireland.

2. That the translator responsible for the attached translation is well acquainted with the German and English languages.

3. That the attached is, to the best of RWS Group plc knowledge and belief, a true translation into the English language of the specification in German filed with the application for a patent in the U.S.A. on **March 26, 2003**

under the number **60/457,810**

4. That I believe that all statements made herein of my own knowledge are true and that all statements made on information and belief are true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the patent application in the United States of America or any patent issuing thereon.

For and on behalf of RWS Group plc

The 22nd day of August 2003

S2359

Digital delay time equalization for parallel data links without a reference line

Description of the technical problem

Memory modules, referred to in the following text as DIMM (dual in-line memory modules) have a defined physical extent. Owing to the finite propagation speed of electrical signals, the physical extent of the DIMM thus corresponds to a delay time for the electrical signal for passing from a source to a sink. This phenomenon is generally referred to as the "line effect", which means that the "electrical length" of the interconnects can no longer be ignored. This is the situation when the highest frequency component which occurs in the signal is at a wavelength which is in the same order of magnitude as the physical extent between the source and the sink.

The higher the data rate on a DIMM, the higher are the frequencies of these frequency components and the shorter are the physical extents for which this line effect must be taken into account. Present-day memory developments are using data rates which, as a result of the described subject, are leading to major time-critical problems. These present memory module developments have the particular characteristic feature of a central integrated circuit (IC) which is mounted on each DIMM. This IC produces the electrical signals for communication with the memory modules locally, that is to say on the DIMM. This basic design is shown in Figure 1. As can be seen, a range of different signals are indicated here, which are either of different

length (DQ/DQS) or else are received simultaneously by a large number of memory modules (CA).

Figure 2 shows the general arrangement, which comprises a central receiver and k transmitting modules. The overall data bus has a width of n bits, so that each transmission module transmits a data bus component of n/k bits. By way of example, the 72 bit data bus of a DIMM of 9 RAM modules can in each case be implemented with an 8 bit data bus component. The described line effects mean that data is subject to different delay times on different interconnects. At the time 1, all n transmitters simultaneously send their data bus component to the receiver. Owing to the different delay times, which are once again based on the different distances from the receiver, the individual data bus components reach the receiver at different times (times 2, 3 and 4). However, parallel data transmission has the characteristic feature that all the information units (bits) which belong to one entire word must reach the receiver within one transmission cycle. This fact would lead to a limitation to the maximum transmission rate on the data bus, since the faster signals would always have to wait for the slower signals before a new transmission cycle can be started.

Figure 3 illustrates the fact of how the integrity of the signals on a parallel data bus is threatened by the different line delay times. As can be seen, the receiver cannot accept the data until, at the earliest, the "data complete" time. This also shows that the maximum data rate is influenced by this. The fastest transmitter must not start to transmit the next data item until all the other (slower) data items have reached the receiver. The new method described in this

document is used to circumvent this limitation to the transmission speed, and nevertheless to ensure the integrity of the data. This is done by using a special algorithm to determine the delay time of the individual signals, which is used for delay time equalization.

Figure 4 illustrates, in principle, the aim of the method. The numbers in the data bits indicate the association, that is to say all "1" bits form a data word, all "2" bits etc. As can be seen, the data line n has a delay of 3UI in comparison to the data line 1 and 2UI in comparison to the data line 2. If the delay time of the individual signals is known, the faster signals can be artificially delayed in the receiver (de-skewing). This is done by an appropriate number (m) of delay elements, which delay each data signal by one clock pulse, and hence by one UI. After this delay, the integrity of the data is ensured once again, with the advantage that the actual transmission rate can be increased considerably.

Previous solutions, disadvantages

One conventional method for compensating for different delay times is for the interconnects to be routed in a meandering shape on the chip. However, this method is quite unsuitable for this application, because the meanders require additional space on the DIMM chip, and this is very short.

A further method defines an additional reference channel with a defined content between the transmitter and receiver. However, since there are a number of receiver modules on one DIMM, this additionally increases the complexity. These known methods are

therefore suitable only to a limited extent for determining and compensating for the delay time of data bits.

New solution, advantages

Once the voltage supply for the DIMM modules has been produced, that is to say once the system has been switched on, there is sufficient time to deal with an initialization routine. Since the described problem results from the physical configuration, that is to say the extent of the arrangement, the effect which must be compensated for is a static effect. Furthermore, all the signal sources and sinks are located in the same module, so that there is no need to take account of any external influences.

The following method determines a discrete value m for each data signal. This value reflects the delay time measured against a fixed defined reference. The following text deals by way of example with a special case, following which this special case will be expanded to the general case.

Once the supply voltage has been switched on, all the transmitters that are involved automatically start to transmit a defined measurement vector. The measurement vector is defined such that it is possible for the receiver to identify a maximum previously defined delay time, and to determine the corresponding value m. For the special case to be investigated, of ±2UI, which must be identified and compensated for, the measurement vector is:

	Sequence 1	**Sequence 2**	**Sequence 3**
Binary	10101010	11001100	11110000
Hexadecimal	AA	CC	F0

Alternatively, the inverted vector can also be used:

Binary	01010101	00110011	00001111
Hexadecimal	33	00	FF

It is irrelevant to the principle which of these two measurement vectors is used. However, the method is described only for the first case. Furthermore, these two vectors represent only the minimum required length for detection and compensation for ±2UI. In principle, the individual sub-sequences can just as well be extended.

This measurement vector is stored in the receiving units for all the data lines in the receiver module. The transmission modules now start to transmit this measurement vector. Depending on the delay time, the measurement vector is received differently. The upper line in each case contains the reference value, and the lower line represents the received data vector.

	Sequence 1	Sequence 2	Sequence 3
• No delay			
Reference	10101010	11001100	11110000
Received	10101010	11001100	11110000
EXOR	00000000	00000000	00000000

• IUI delay			
Reference	10101010	11001100	11110000
Received	?1010101	01100110	01111000
EXOR	?1111111	10101010	10001000

• 2UI delay			
Reference	10101010	11001100	11110000
Received	??101010	10110011	00111100
EXOR	??000000	01111111	11001100

• IUI advance			
Reference	10101010	11001100	11110000
Received	01010101	10011001	1110000?
EXOR	11111111	01010101	0001000?

• 2UI advance			
Reference	10101010	11001100	11110000
Received	10101011	00110011	110000??
EXOR	00000001	11111111	001100??

The evaluation is carried out in two steps. First of all, it is necessary to identify whether there is any shift, that is to say a 0.1 or 2 UI shift in comparison to the reference vector. The direction must be determined in a second step, that is to say whether this is a delay or an advance (see the examples above).

The presence of a shift can occur by means of a simple EXOR gate logic operation on the reference and data vectors. Each shift depth is addressed by its own sequence. The sequence 1 is used to identify a 1UI shift, the sequence 2 to identify a 2UI shift, etc. As can be seen from the above examples, a permanent "1" is produced at the output of the EXOR only for the

respective sequence. In this case, it is irrelevant whether this is a delay or an advance, the fact that a shift has occurred is reliably determined using this method.

A delay is distinguished by the fact that all the data changes, that is to say 1-0 transitions and 0-1 transitions, occur first of all in the reference vector and only later in the delayed data vector. An advance can be identified by the opposite condition, that is to say a data change occurs in the data vector first of all and then in the reference vector. Transitions can be identified by an edge detector as shown in the arrangement in Figure 5. The direction, that is to say the time sequence of the transitions, can be determined by the extended arrangement shown in Figure 6.

The sequence which follows the identification sequence is used to determine the shift direction. The sequence 2 gives the associated direction for the example of a 1UI delay. This is also the reason why three sequences are necessary to reliably identify ±2UI. Although the sequence 2 itself reliably detects the presence of a shift of 2UI, the sequence 3 is, however, required in order to determine the associated direction.

The general case will now be defined in order to cover all the measurement vectors used for this purpose. It is assumed that a maximum shift of ±mUI is to be identified and compensated for. The measurement vectors can best be regarded as a field comprising a number of line vectors. The line vectors are characterized in that the data rate is halved from one line to the next. For the situation mentioned above (±2UI), the field of the reference vector would therefore be:

10101010
11001100
11110000

The field therefore comprises 3 lines, and each line has a length of 8 bits. The general field for compensation for ±mUI has AZ lines, where AZ is defined as:

$$AZ = \text{ceil}\left(\frac{\log 2m}{\log 2}\right)+1$$

"ceil" is a rounding function, which produces an integer value by rounding up. The length of the lines (LZ) is defined by: $LZ = 2^{AZ}$

A field for compensation for ±4UI would therefore comprise AZ = 4 lines, each having $2^4 = 16$ bits. The associated field is then:

10101010 10101010
11001100 11001100
11110000 11110000
11111111 00000000

Advantages

- Additional delay times within the module, for example in data recovery or during multiplexing/demultiplexing, need no longer be dealt with separately, but are covered automatically by the algorithm.

Essence of the Invention

The fundamental principle is the special data vector which is transmitted by each module. The creation of the vector has already been described in detail above. The fact that the data rate of the vector is halved from one line to the next, that is to say from one sequence to the next, is particularly important. The line of vectors thus produce a counting system, which could also identify additive delays, that is to say 3, 5 UI etc. Furthermore, all the transmission modules and the receiver modules must have the same measurement vector in order to make it possible to carry out the measurement in this way.

Verification of use in competitive products

Use can be verified only by non-destructive measurement on competitive products. If a measurement vector such as this has been used from the start, then the only conclusion that can be drawn from this is that this is a delay time compensation method.